ECE2883 HP – T. Collins, Fall 2015

Hardware interconnection for DE2-115

Introduction

This document addresses the DE2-115 and the primary daughterboard, as shown in Figure 1. This photograph also shows the I/O breakout board (top of the stack), but it is possible that no project teams will need it, so it is not currently discussed here. The I/O breakout board supports the LED arrays (not being used), the light projector (not being used), audio amplifiers for audio transducers (possibly being used, but it is probably easier to treat audio transducers like solenoids), and an Arduino shield for bidirectional motor control (probably not being used).

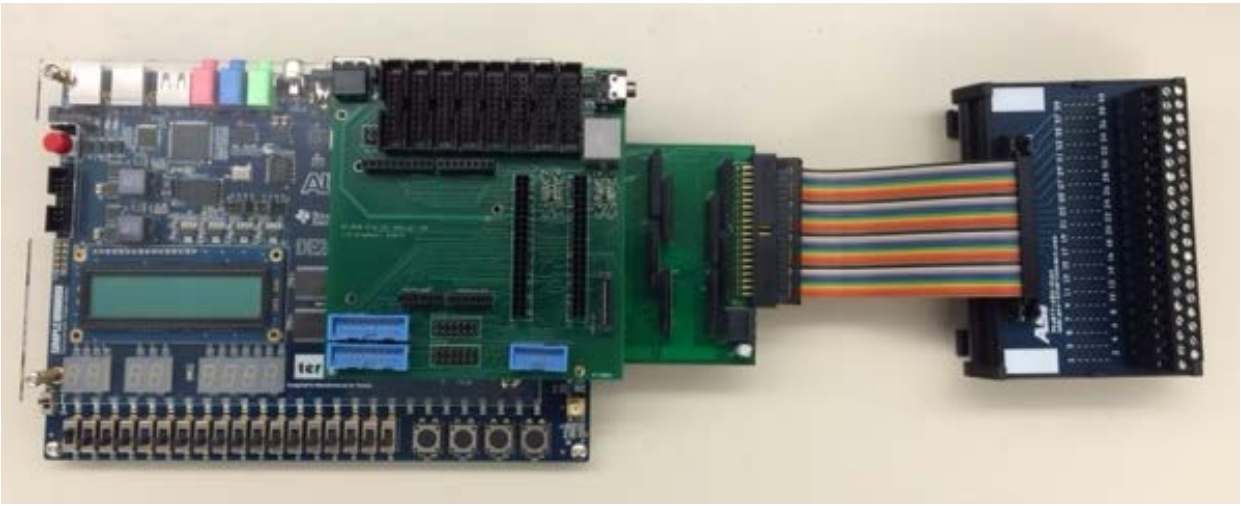

Figure 1. DE2-115 with daughterboard, I/O breakout board, and attached terminal block.

Daughterboard

An overview illustration of the DE2-115 daughterboard is shown in Figure 2. The daughterboard must be centered with its JP1 connector mating exactly with the JP1 connector of the DE2-115. When this is done correctly, another adjoining connector (on underside of board below JP2) will mate exactly with a high-density connector on the DE2-115, making dozens more signals available for use.

Power connections

The two-pin connectors TB1 and TB2 are used to bring power to the board, since the DE2-115 power supply cannot provide enough current for most of our needs in ECE2883HP.

- Most teams need a power supply connected to TB1, supplying the power needed for devices connected to the high-current Darlington outputs. It can be 5 V or 12 V, depending on the needs of the connected devices. If you have some devices that require 5 V and others that require 12 V, use TB1 for the 5 V power connection, and make 12 V connections DIRECTLY TO THE DEVICES (ask Dr. Collins or Kevin for assistance).

- Small solenoids require 5 V
- Large solenoids require 12 V
- Audio transducers require 5 V
- DC motors (other than RC servos) may require 5 V or 12 V
- LED lighting strips require 12 V
- Servos, lasers, and other devices are NOT connected to the high-current Darlington outputs, so they have no impact on the power connected to TB1.

TB2: Any team that is using a Trellis keyboard should connect 5 V to TB2, and the jumper JP4 should be set with pins 2 and 3 connected (the bottom pair of pins).

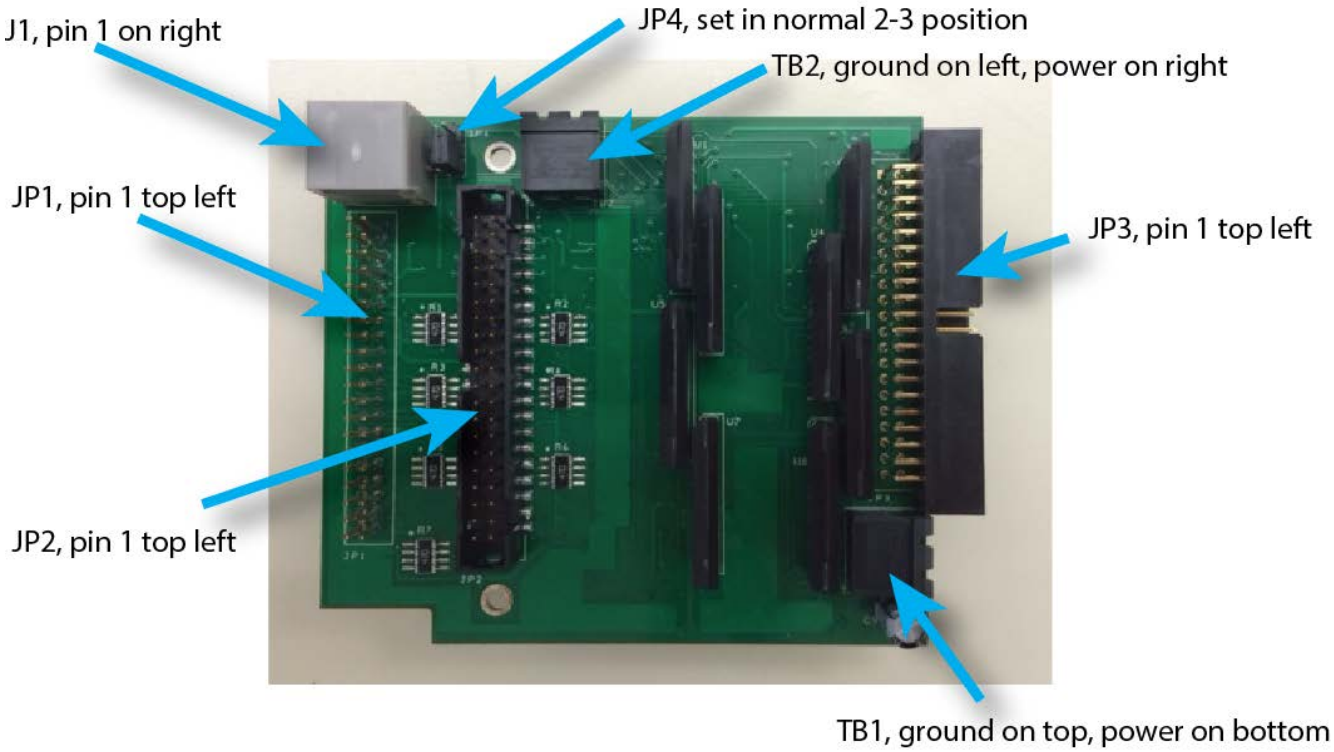

Figure 2. DE2-115 daughterboard created to bring out more pins for student use. All references to right/left are relative to right and left of this view (i.e., NOT looking into the connector).

Power needs

If you are using a small wall transformer to connect to TB1 or TB1, like the one you probably received when you got your boards, bear in mind that they only put out enough current for a couple small solenoids or motors. Ask for a bigger power supply as you build up hardware, and allow an area in your design to mount it (roughly 8” x 6” x 2” for a 12 V supply, and a little thinner for a 5 V supply).

High-current device connection

JP3 (see Figure 2 for location) provides pins to connect up to 32 devices that require "high current," anything other than something that is logic-compatible. This is implemented with 32 pins that "pull down" one pin of the connected device, drawing up to 2 A of current to ground. The other pin of the connected device must be connected to a power supply (see the previous section about the use of TB1 to get that power into the board). As shown on the right side of Figure 3, that power is available on six pins of JP3, for direct connection to high-current devices. The remaining pins of JP3 are driven by FPGA pins through Darlington transistor drivers, as listed in Table 1 below.

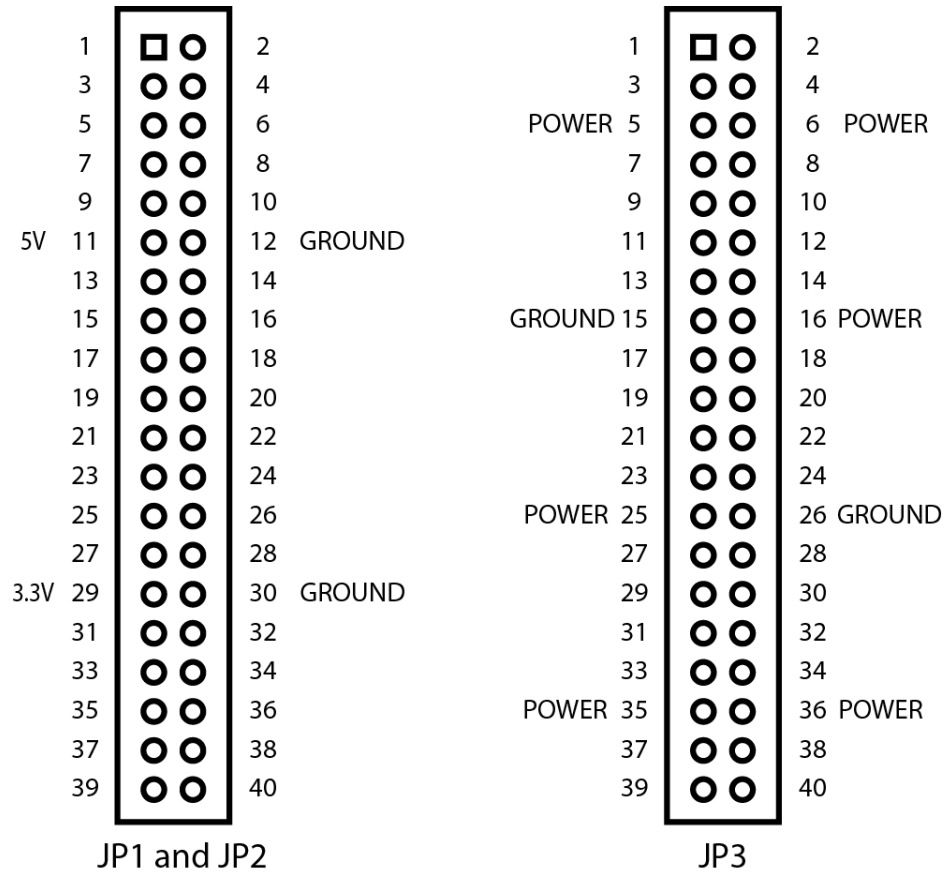

Figure 3. Forty-pin connectors on Daughterboard, as viewed from entering the connector (top of JP1 and JP2, right side of JP3). Every pin not shown as power or ground is available as a digital input or output (low current on JP1 and JP2, high current on JP3).

The terminal block on the right side of the photo in Figure 1 is very useful for connecting devices to JP3. When connected to JP3 with a ribbon cable as shown (pin 1 of JP3 to pin 1 of ribbon cable, and then pin 1 of ribbon cable to terminal block pin 1), the pin labels on the terminal block will correspond exactly to the numbers in Figure 3 and Table 1, so it will be relatively easy to connect both power and signals to solenoids and other high current devices. The same power terminal (such as pin 5 on the terminal block) can be used for ONE wire of multiple high-current devices, but the OTHER wire of each high-current device will have its own pin such as HCIO[0], HCIO[1], etc.

Table 1: Pin assignments for high-current signals on JP3,

Pin Number	Pin Name	FPGA Pin
1	HCIO[0]	PIN_AE26
2	HCIO[1]	PIN_L23
3	HCIO[2]	PIN_AE27
4	HCIO[3]	PIN_AE28
7	HCIO[4]	PIN_D27
8	HCIO[5]	PIN_AF27
9	HCIO[6]	PIN_D28
10	HCIO[7]	PIN_F24
11	HCIO[8]	PIN_K21
12	HCIO[9]	PIN_L24
13	HCIO[10]	PIN_K22
14	HCIO[11]	PIN_M25
17	HCIO[12]	PIN_H23
18	HCIO[13]	PIN_F25
19	HCIO[14]	PIN_H24
20	HCIO[15]	PIN_M26

Pin Number	Pin Name	FPGA Pin
21	HCIO[16]	PIN_R27
22	HCIO[17]	PIN_P25
23	HCIO[18]	PIN_R28
24	HCIO[19]	PIN_P26
27	HCIO[20]	PIN_U27
28	HCIO[21]	PIN_P21
29	HCIO[22]	PIN_U28
30	HCIO[23]	PIN_R21
31	HCIO[24]	PIN_V27
32	HCIO[25]	PIN_R22
33	HCIO[26]	PIN_V28
34	HCIO[27]	PIN_R23
37	HCIO[28]	PIN_U22
38	HCIO[29]	PIN_T21
39	HCIO[30]	PIN_V22
40	HCIO[31]	PIN_T22

Low-current device connection

Headers JP1 and JP2 are available for general use as logic inputs or outputs. Collectively, these signals are called GPIO, and the ones on JP1 are named GPIO_0[0] through GPIO_0[35], while the ones on JP2 are named GPIO_1[0] through GPIO_1[35]. A list of all signals is given in Table 1.

They can be connected to switches, RC servos, and lasers. In the case of switches, one wire of the switch should be connected to a 5 V source through a resistor of about 1 kOhm, and the other wire would be connected to a GPIO pin, configured as an input to the FPGA. In the case of an RC servo or laser, there is a ground wire (usually black) and a power wire (usually red) that must be connected to a power supply. The third wire (yellow or white) is the one that should be connected to a GPIO pin, configured as an output from the FPGA.

Refer to the previous section for a discussion of the terminal block, shown on the right of Figure 1. Another one can be used to connect to JP1 or JP2, in much the same way. Consult with Dr. Collins or Kevin before relying on the 5 V power on JP1 or JP2, however, since it comes from the DE2 board and it may not be sufficient for your needs.

Other connections

The grey J1 connector is used for a custom cable that can be connected to up to 8 Trellis keypads. Connectors on the DE2-115 may be needed for some specific applications. See the DE2 manual for details. These pins, as well as assignments for devices on the DE2-115 (such as numeric displays, switches, and LEDS) are listed below in Table 3. Many DE2-115 functions have been omitted here, but again, the DE2 manual has additional information if needed.

Table 2: Pin assignments for low-current signals on JP1 and JP2.

Connector Pin	Connector JP1 usage		Connector JP2 usage	
	Name	FPGA pin	Name	FPGA pin
1	GPIO_0[0]	PIN_AB22	GPIO_1[0]	PIN_D26
2	GPIO_0[1]	PIN_AC15	GPIO_1[1]	PIN_G26
3	GPIO_0[2]	PIN_AB21	GPIO_1[2]	PIN_C27
4	GPIO_0[3]	PIN_Y17	GPIO_1[3]	PIN_G25
5	GPIO_0[4]	PIN_AC21	GPIO_1[4]	PIN_E27
6	GPIO_0[5]	PIN_Y16	GPIO_1[5]	PIN_E26
7	GPIO_0[6]	PIN_AD21	GPIO_1[6]	PIN_E28
8	GPIO_0[7]	PIN_AE16	GPIO_1[7]	PIN_F26
9	GPIO_0[8]	PIN_AD15	GPIO_1[8]	PIN_F27
10	GPIO_0[9]	PIN_AE15	GPIO_1[9]	PIN_H25
13	GPIO_0[10]	PIN_AC19	GPIO_1[10]	PIN_F28
14	GPIO_0[11]	PIN_AF16	GPIO_1[11]	PIN_H26
15	GPIO_0[12]	PIN_AD19	GPIO_1[12]	PIN_G27
16	GPIO_0[13]	PIN_AF15	GPIO_1[13]	PIN_K25
17	GPIO_0[14]	PIN_AF24	GPIO_1[14]	PIN_G28
18	GPIO_0[15]	PIN_AE21	GPIO_1[15]	PIN_K26
19	GPIO_0[16]	PIN_AF25	GPIO_1[16]	PIN_K27
20	GPIO_0[17]	PIN_AC22	GPIO_1[17]	PIN_R25
21	GPIO_0[18]	PIN_AE22	GPIO_1[18]	PIN_K28
22	GPIO_0[19]	PIN_AF21	GPIO_1[19]	PIN_R26
23	GPIO_0[20]	PIN_AF22	GPIO_1[20]	PIN_M27
24	GPIO_0[21]	PIN_AD22	GPIO_1[21]	PIN_T25
25	GPIO_0[22]	PIN_AG25	GPIO_1[22]	PIN_M28
26	GPIO_0[23]	PIN_AD25	GPIO_1[23]	PIN_T26
27	GPIO_0[24]	PIN_AH25	GPIO_1[24]	PIN_J25
28	GPIO_0[25]	PIN_AE25	GPIO_1[25]	PIN_U25
31	GPIO_0[26]	PIN_AG22	GPIO_1[26]	PIN_J26
32	GPIO_0[27]	PIN_AE24	GPIO_1[27]	PIN_U26
33	GPIO_0[28]	PIN_AH22	GPIO_1[28]	PIN_L27
34	GPIO_0[29]	PIN_AF26	GPIO_1[29]	PIN_L21
35	GPIO_0[30]	PIN_AE20	GPIO_1[30]	PIN_L28
36	GPIO_0[31]	PIN_AG23	GPIO_1[31]	PIN_L22
37	GPIO_0[32]	PIN_AF20	GPIO_1[32]	PIN_V25
38	GPIO_0[33]	PIN_AH26	GPIO_1[33]	PIN_N25
39	GPIO_0[34]	PIN_AH23	GPIO_1[34]	PIN_V26
40	GPIO_0[35]	PIN_AG26	GPIO_1[35]	PIN_N26

Table 3. Other pin assignments of possible interest.

FPGA Pin	Usage	Physical Connector and Pin
PIN_P27	KEYPAD1_INT	J1-5
PIN_J24	KEYPAD1_SCL	J1-2
PIN_J23	KEYPAD1_SDA	J1-1
PIN_P28	KEYPAD1_SPARE	J1-6

FPGA Pin	Usage	Physical Connector and Pin
PIN_Y2	CLOCK_50	On DE2
PIN_AG14	CLOCK2_50	On DE2
PIN_AG15	CLOCK3_50	On DE2
PIN_J10	EX_IO[0]	On DE2
PIN_J14	EX_IO[1]	On DE2
PIN_H13	EX_IO[2]	On DE2
PIN_H14	EX_IO[3]	On DE2
PIN_F14	EX_IO[4]	On DE2
PIN_E10	EX_IO[5]	On DE2
PIN_D9	EX_IO[6]	On DE2
PIN_G18	HEX0[0]	On DE2
PIN_F22	HEX0[1]	On DE2
PIN_E17	HEX0[2]	On DE2
PIN_L26	HEX0[3]	On DE2
PIN_L25	HEX0[4]	On DE2
PIN_J22	HEX0[5]	On DE2
PIN_H22	HEX0[6]	On DE2
PIN_M24	HEX1[0]	On DE2
PIN_Y22	HEX1[1]	On DE2
PIN_W21	HEX1[2]	On DE2
PIN_W22	HEX1[3]	On DE2
PIN_W25	HEX1[4]	On DE2
PIN_U23	HEX1[5]	On DE2
PIN_U24	HEX1[6]	On DE2
PIN_AA25	HEX2[0]	On DE2
PIN_AA26	HEX2[1]	On DE2
PIN_Y25	HEX2[2]	On DE2
PIN_W26	HEX2[3]	On DE2
PIN_Y26	HEX2[4]	On DE2
PIN_W27	HEX2[5]	On DE2
PIN_W28	HEX2[6]	On DE2
PIN_V21	HEX3[0]	On DE2
PIN_U21	HEX3[1]	On DE2
PIN_AB20	HEX3[2]	On DE2
PIN_AA21	HEX3[3]	On DE2
PIN_AD24	HEX3[4]	On DE2
PIN_AF23	HEX3[5]	On DE2
PIN_Y19	HEX3[6]	On DE2
PIN_AB19	HEX4[0]	On DE2
PIN_AA19	HEX4[1]	On DE2
PIN_AG21	HEX4[2]	On DE2
PIN_AH21	HEX4[3]	On DE2

FPGA Pin	Usage	Physical Connector and Pin
PIN_AE19	HEX4[4]	On DE2
PIN_AF19	HEX4[5]	On DE2
PIN_AE18	HEX4[6]	On DE2
PIN_AD18	HEX5[0]	On DE2
PIN_AC18	HEX5[1]	On DE2
PIN_AB18	HEX5[2]	On DE2
PIN_AH19	HEX5[3]	On DE2
PIN_AG19	HEX5[4]	On DE2
PIN_AF18	HEX5[5]	On DE2
PIN_AH18	HEX5[6]	On DE2
PIN_AA17	HEX6[0]	On DE2
PIN_AB16	HEX6[1]	On DE2
PIN_AA16	HEX6[2]	On DE2
PIN_AB17	HEX6[3]	On DE2
PIN_AB15	HEX6[4]	On DE2
PIN_AA15	HEX6[5]	On DE2
PIN_AC17	HEX6[6]	On DE2
PIN_AD17	HEX7[0]	On DE2
PIN_AE17	HEX7[1]	On DE2
PIN_AG17	HEX7[2]	On DE2
PIN_AH17	HEX7[3]	On DE2
PIN_AF17	HEX7[4]	On DE2
PIN_AG18	HEX7[5]	On DE2
PIN_AA14	HEX7[6]	On DE2
PIN_M23	KEY[0]	On DE2
PIN_M21	KEY[1]	On DE2
PIN_N21	KEY[2]	On DE2
PIN_R24	KEY[3]	On DE2
PIN_L6	LCD_BLON	On DE2
PIN_L3	LCD_DATA[0]	On DE2
PIN_L1	LCD_DATA[1]	On DE2
PIN_L2	LCD_DATA[2]	On DE2
PIN_K7	LCD_DATA[3]	On DE2
PIN_K1	LCD_DATA[4]	On DE2
PIN_K2	LCD_DATA[5]	On DE2
PIN_M3	LCD_DATA[6]	On DE2
PIN_M5	LCD_DATA[7]	On DE2
PIN_L4	LCD_EN	On DE2
PIN_L5	LCD_ON	On DE2
PIN_M2	LCD_RS	On DE2
PIN_M1	LCD_RW	On DE2
PIN_E21	LEDG[0]	On DE2

FPGA Pin	Usage	Physical Connector and Pin
PIN_E22	LEDG[1]	On DE2
PIN_E25	LEDG[2]	On DE2
PIN_E24	LEDG[3]	On DE2
PIN_H21	LEDG[4]	On DE2
PIN_G20	LEDG[5]	On DE2
PIN_G22	LEDG[6]	On DE2
PIN_G21	LEDG[7]	On DE2
PIN_F17	LEDG[8]	On DE2
PIN_G19	LEDR[0]	On DE2
PIN_F19	LEDR[1]	On DE2
PIN_J15	LEDR[10]	On DE2
PIN_H16	LEDR[11]	On DE2
PIN_J16	LEDR[12]	On DE2
PIN_H17	LEDR[13]	On DE2
PIN_F15	LEDR[14]	On DE2
PIN_G15	LEDR[15]	On DE2
PIN_G16	LEDR[16]	On DE2
PIN_H15	LEDR[17]	On DE2
PIN_E19	LEDR[2]	On DE2
PIN_F21	LEDR[3]	On DE2
PIN_F18	LEDR[4]	On DE2
PIN_E18	LEDR[5]	On DE2
PIN_J19	LEDR[6]	On DE2
PIN_H19	LEDR[7]	On DE2
PIN_J17	LEDR[8]	On DE2
PIN_G17	LEDR[9]	On DE2
PIN_AB28	SW[0]	On DE2
PIN_AC28	SW[1]	On DE2
PIN_AC24	SW[10]	On DE2
PIN_AB24	SW[11]	On DE2
PIN_AB23	SW[12]	On DE2
PIN_AA24	SW[13]	On DE2
PIN_AA23	SW[14]	On DE2
PIN_AA22	SW[15]	On DE2
PIN_Y24	SW[16]	On DE2
PIN_Y23	SW[17]	On DE2
PIN_AC27	SW[2]	On DE2
PIN_AD27	SW[3]	On DE2
PIN_AB27	SW[4]	On DE2
PIN_AC26	SW[5]	On DE2
PIN_AD26	SW[6]	On DE2
PIN_AB26	SW[7]	On DE2

FPGA Pin	Usage	Physical Connector and Pin
PIN_AC25	SW[8]	On DE2
PIN_AB25	SW[9]	On DE2
PIN_B7	I2C_SCLK	On DE2
PIN_A8	I2C_SDAT	On DE2
PIN_G12	UART_RXD	On DE2
PIN_G9	UART_TXD	On DE2
PIN_G14	UART_CTS	On DE2
PIN_J13	UART_RTS	On DE2
PIN_G6	PS2_CLK	On DE2
PIN_H5	PS2_DAT	On DE2
PIN_G5	PS2_CLK2	On DE2
PIN_F5	PS2_DAT2	On DE2